Thermal Isolation and Differential Cooling of Heterogeneously Integrated Devices

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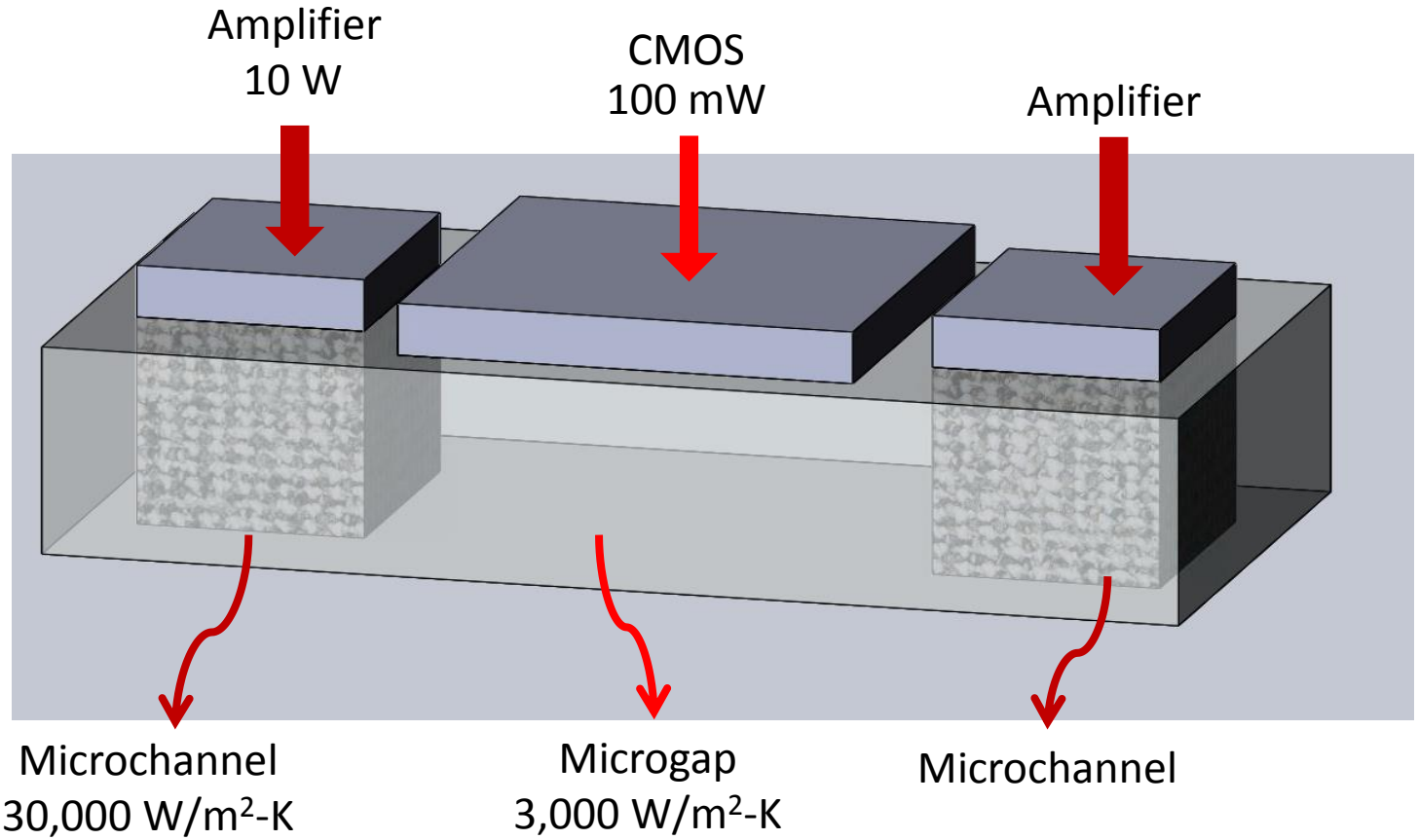
Overall Goal of the Program

Permit heterogeneous integration of power and logic devices with minimum separation in SiP/SoC configuration by

- Providing sufficient cooling of high power dissipating devices, while also
- Providing thermal isolation to temperature sensitive devices using a combination of the following:
  - Low conductivity Interposer (< 25 W/m-K)
    - Glass, Al_2O_3, (and Silicon baseline)
  - High conductivity thermal interconnects (> 250 W/m-K)
    - Through-layer-via (TXV) arrays
    - Cu filled vias, Cu conformal vias, Cu frit filled vias
  - Site specific differential cooling
    - Microfluidic (3,000 W/m^2-K v. 30,000 W/m^2-K)
    - Thermoelectric

Chiplet on Substrate

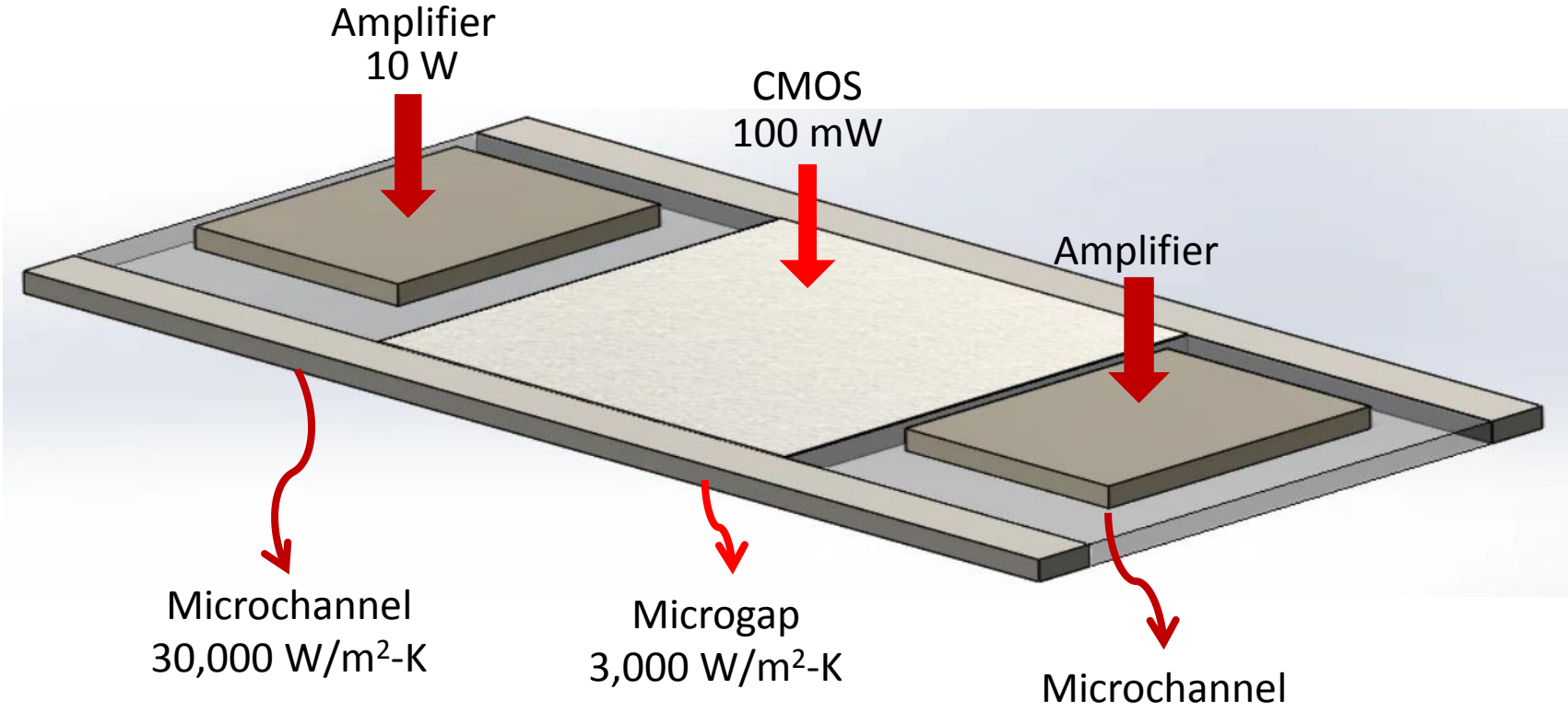
Low and high power dissipating chiplets located on a common low conductivity substrate with TXV and microchannel cooling under higher flux areas.



GOAL: Examine temperature rise of individual chips (e.g. CMOS) from heat generated by power amplifier chip

Chiplet on Chip

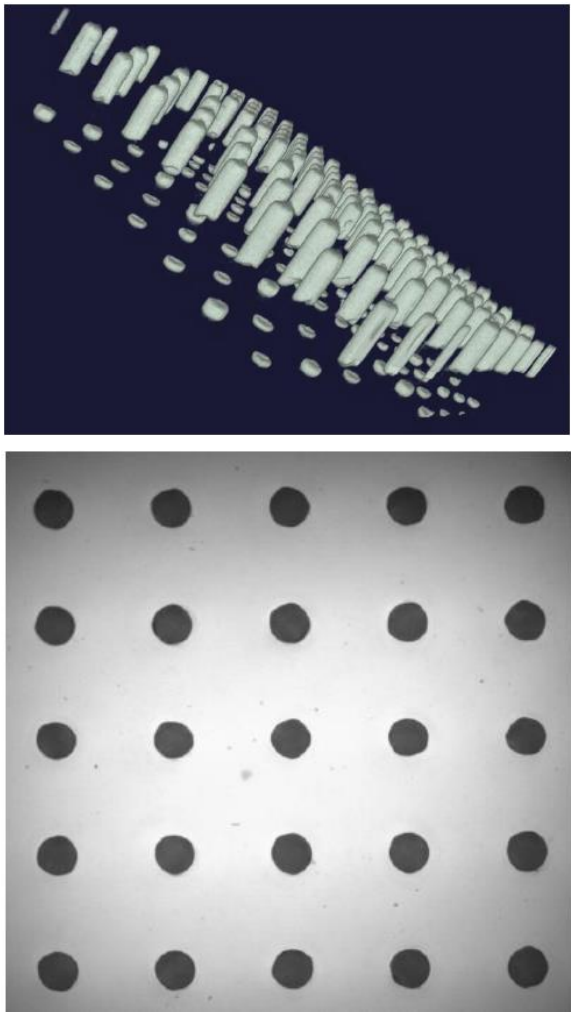
CMOS device is patterned on base silicon wafer. High power dissipating chiplets are placed on via-enhanced low-k material deposited on base wafer and joined to differential cooling.



GOAL: Examine thermal isolation of heterogeneous SoC systems

Thermal Via Arrays

- Through-layer vias (TXVs) are an accessible tool for inserting thermal pathways within a die or device package
- Regular arrays of vias result in a composite thermal material with unique, tunable properties
  - Co-opted for electrical interconnection
  - Anisotropic behavior used for thermal isolation
- Homogenization: set of modeling techniques where the full-detail array is approximated with an equivalent, homogeneous medium

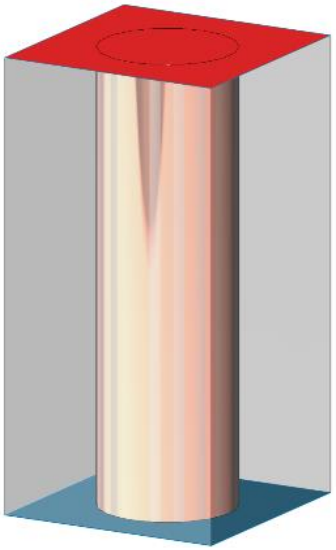


Top: 3D X-ray CT scan of 50 µm TSV array. Sekhar, *et al* (EPTC 2010)
Bottom: 30 µm through-hole array in glass interposer. Shorey, *et al* (ECTC 2012)

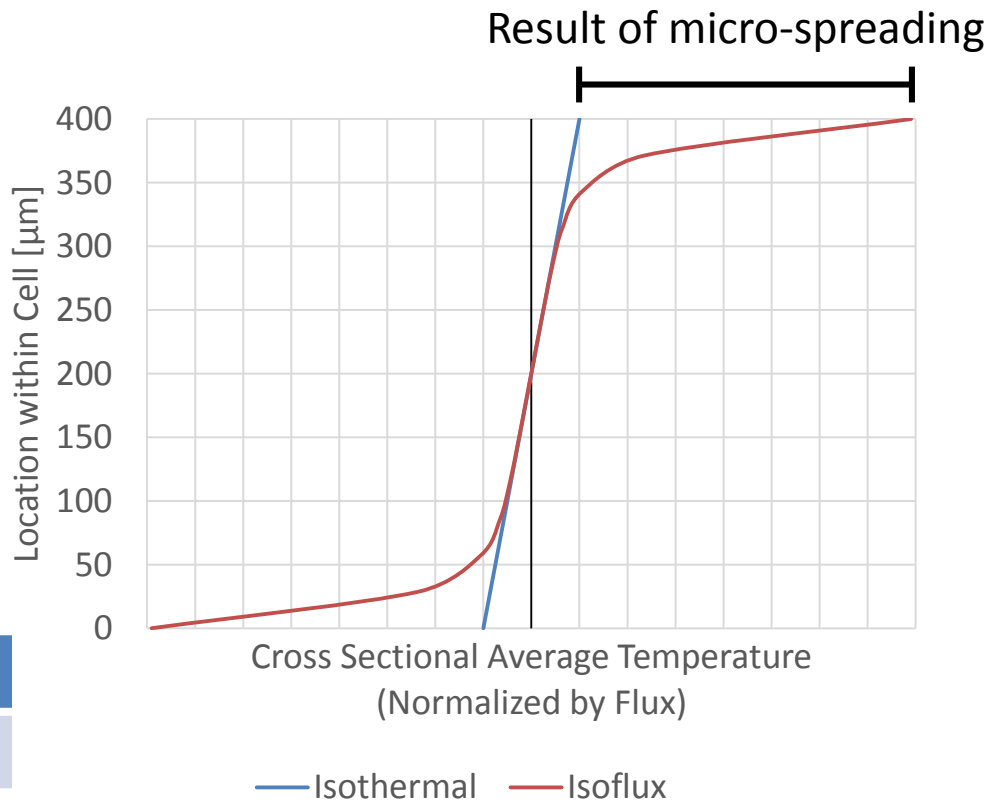
Micro-Spreading Resistance

Two vias with the same properties exhibit different behavior when subjected to different boundary conditions

- A cell with isothermal boundaries compared to one with isoflux ones

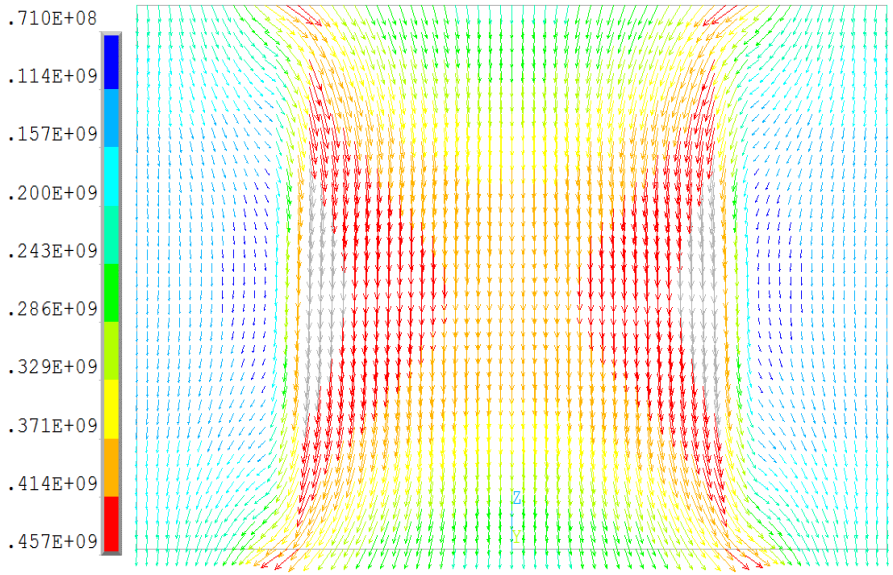


k_v	k_s	d_v	P
400	1	60 µm	100 µm



Micro-Spreading Resistance and $k_{eff,z}$

- The thermal performance of a TXV array relies on its ability to transmit heat through the interposer layer
- Non-uniform temperatures at interposer surfaces lead to lateral heat flux components, resulting in a micro-spreading resistance
- This resistance, existing at the via scale, is in addition to any system level macro-spreading (i.e. thermal constriction) resistances

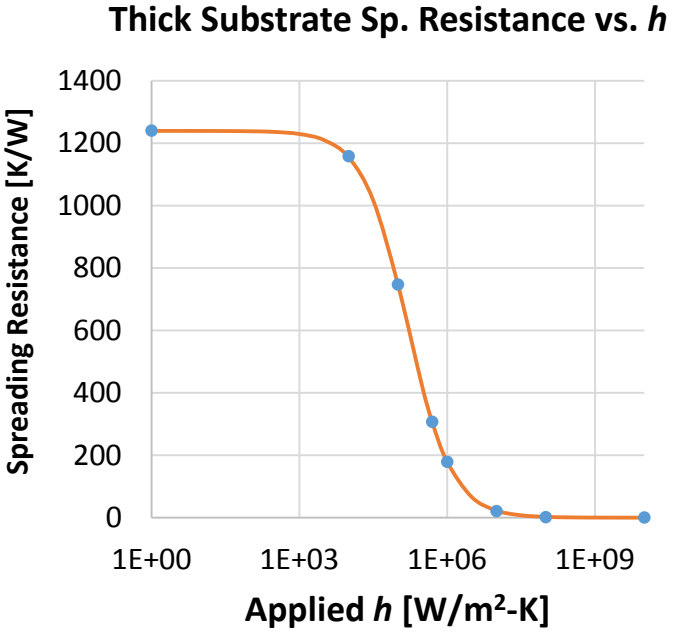


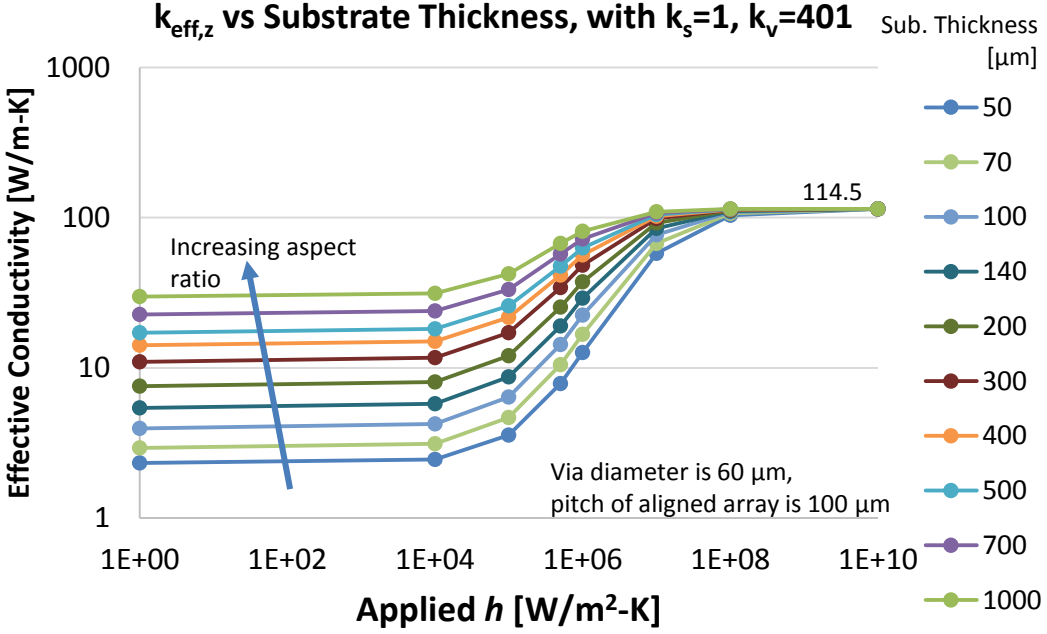
- The increase in thermal resistance due to micro-spreading can be addressed by assigning the material an effective thermal conductivity.

$$k_{eff,z} = \frac{L}{A(R_{1D}+R_{sp})}$$

- This allows the more complicated via array to be modeled using an equivalent homogeneous medium

Micro-Spreading Resistance and $k_{eff,z}$

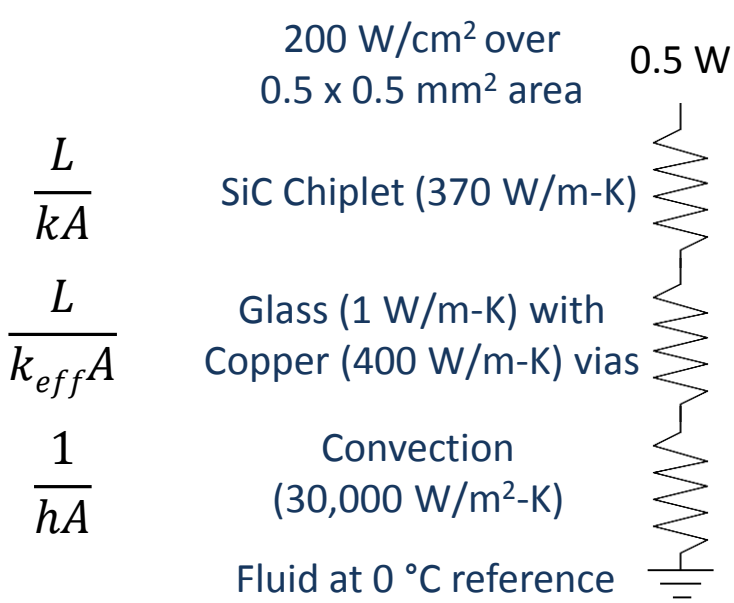


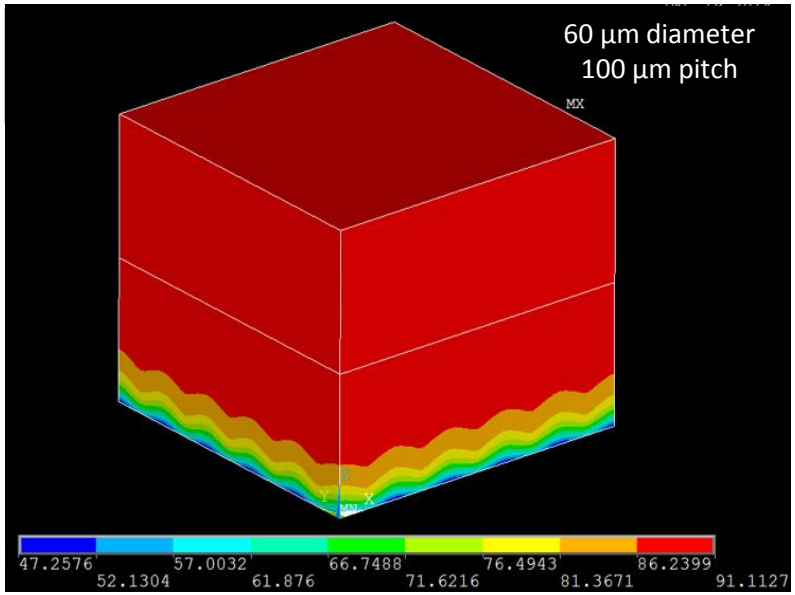


- Thermal boundary conditions play a large role in the spreading resistance of a via array.
- Because spreading resistance doesn't change as the length of the vias increases, high aspect vias have higher k_{eff}
- The maximum conductivity possible is the rule-of-mixtures, when $R_{sp} = 0$
- This happens when the surfaces of the interposer have uniform temperatures

1D Analysis for Different Via Geometries

- Consider 3 via array geometries, with the same 28% Cu fill factor.
- A simple system with constant cross section allows comparison with a 1D analysis
- A rule-of-mixtures for 28% Cu would predict a 3.5 °C drop across the interposer

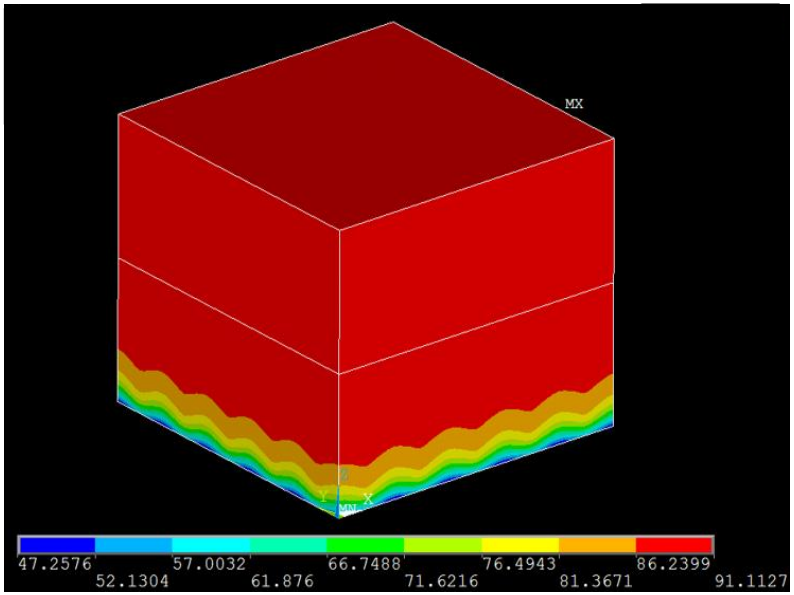




All layers are 200 µm thick

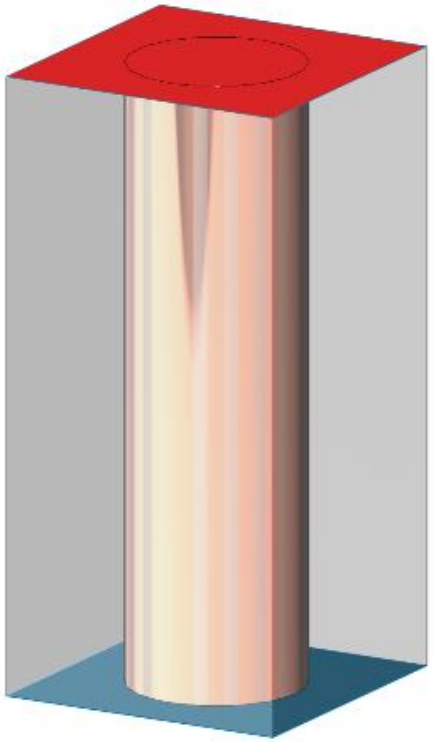
1D Analysis for Different Via Geometries

- The temperature at the bottom interposer surface is non-uniform
- At the top interposer surface, the uniformity is to within 1 °C
- An average temperature difference is defined across each layer

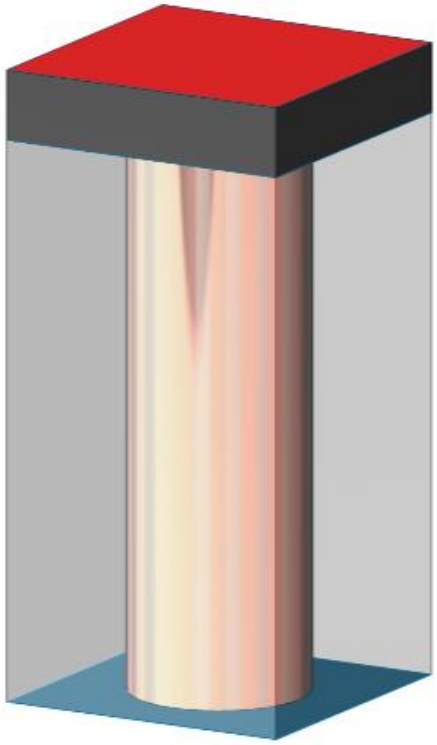


Q: 0.5 W	ΔT_{avg} Case 1 [°C] 30 µm at 50 µm	ΔT_{avg} Case 2 [°C] 60 µm at 100 µm	ΔT_{avg} Case 3 [°C] 150 µm at 250 µm
SiC	~ 1	~ 1	~ 1
Interposer	15	24	45
Convection	66	66	66
Total Temp Rise	**82**	**91**	**112**

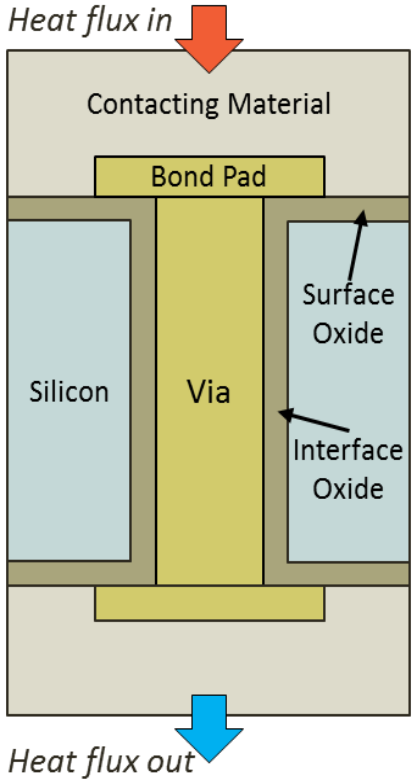
Via Cell Used for Modeling



Glass unit cell containing filled copper via

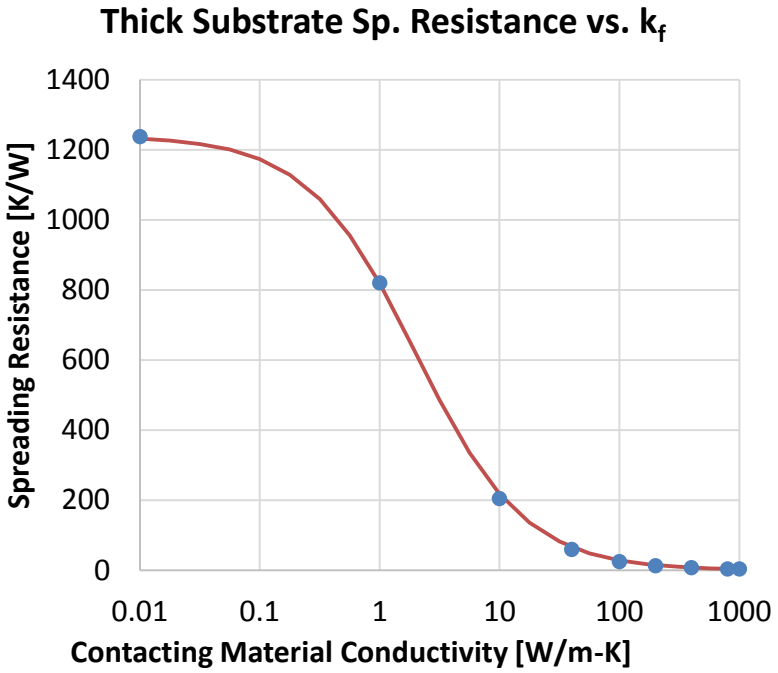


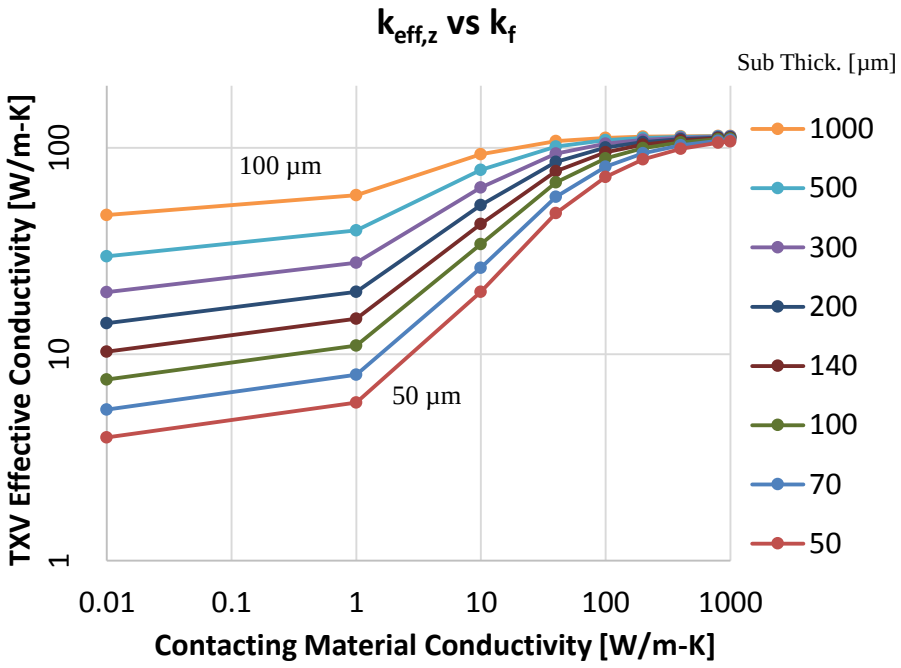
Glass unit cell containing filled copper via and heat spreading film on top



TGV results may also be leveraged to understand TSV

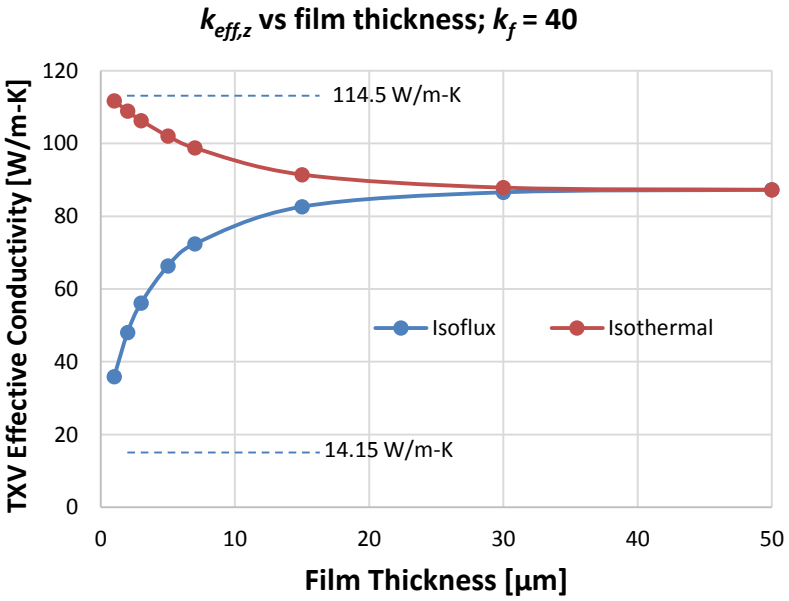
Micro-Spreading and Materials





- Micro-spreading exists when heat flows from a uniform material into the via array
- This resistance is most important when contacting low thermal conductivity materials.
  - Die attach materials, organics in back-end-of-line or redistribution layers

Effect of Film on 1D Chip Temperature

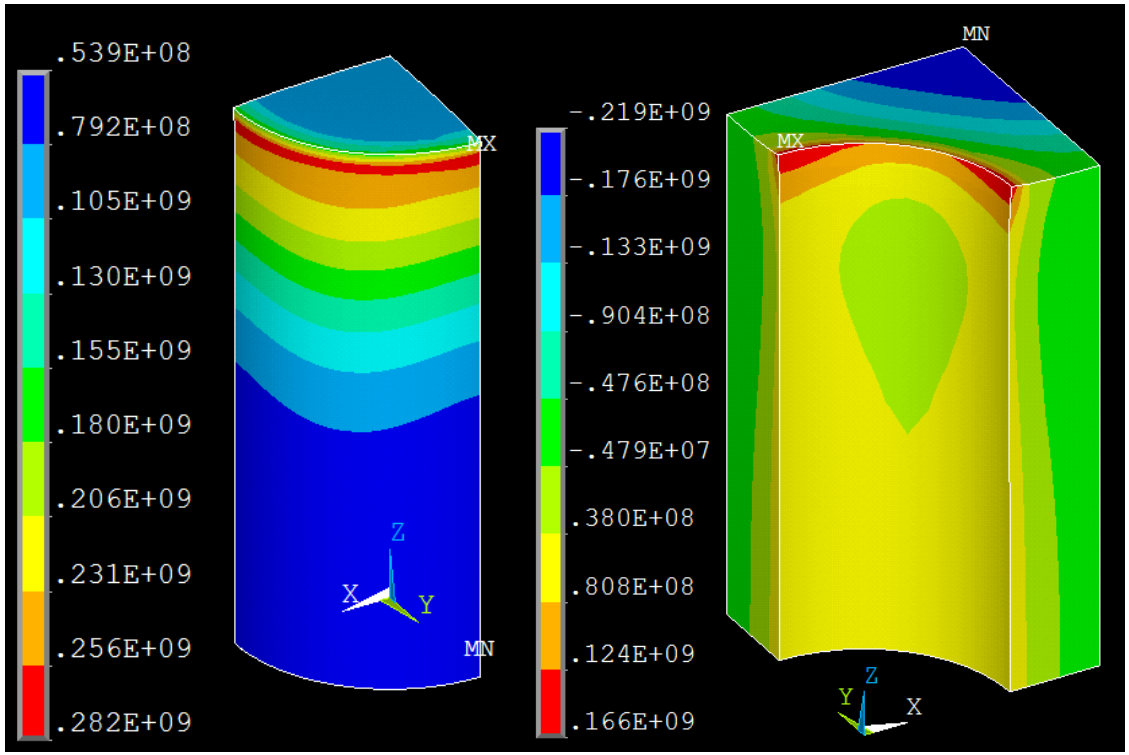


- Adding a copper film dramatically reduces the spreading resistance at the fluid interface
- It eases the transition between the convection boundary and the bulk of the interposer.
- Going back to Case 3, the optimal film thickness is close to 15 µm.

ΔT_{avg} by layer	ΔT_{avg} Case 3 [K]	ΔT_{avg} [K] 6 µm film	ΔT_{avg} [K] 15 µm film	ΔT_{avg} [K] 25 µm film
SiC	~ 1	1.08	1.08	1.08
Interposer	45	3.98	3.84	3.81
Film	~	0.03	0.08	0.13
Convection	66	66.66	66.66	66.66
Film + Int ΔT	**45**	**4.01**	**3.92**	**3.94**

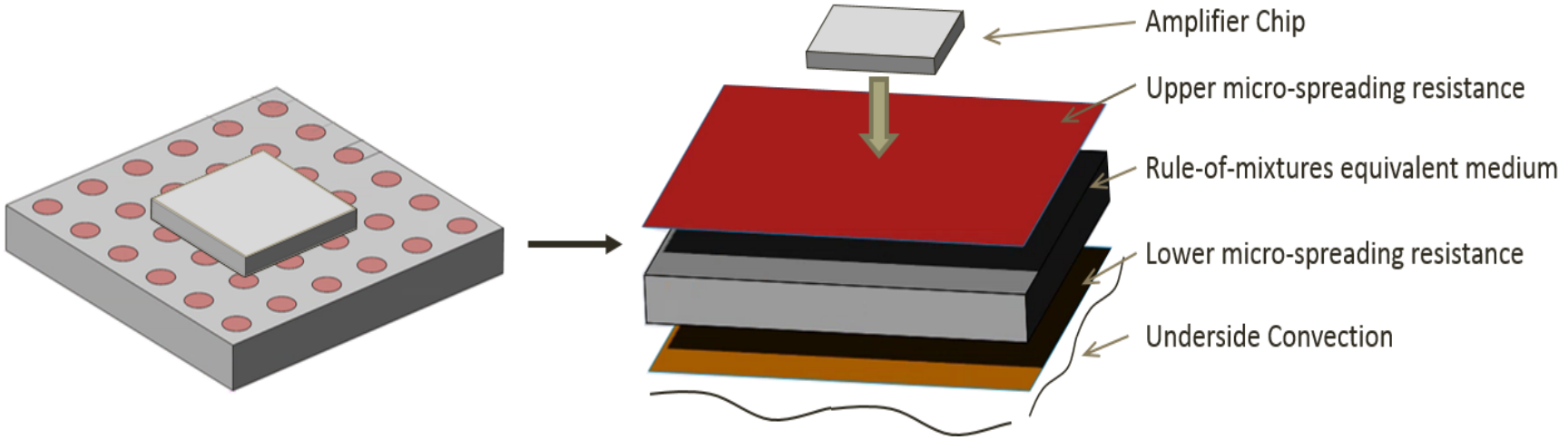
Structural Reliability Modeling

- Thermal stress modeling is used to identify via array materials and dimensions that will have reliability concerns.
- Possible failure modes are:
  - Fatigue failure of ductile via material (via extrusion)
  - Interfacial delamination between via and substrate
  - Brittle substrate crack growth
- Trade-offs between reliability and thermal performance are being considered.
- For this case, at a hoop stress of 166 MPa in glass with a K_{IC} of 0.7 MPa$\sqrt{m}$, the critical crack size is > 5.6 μm.



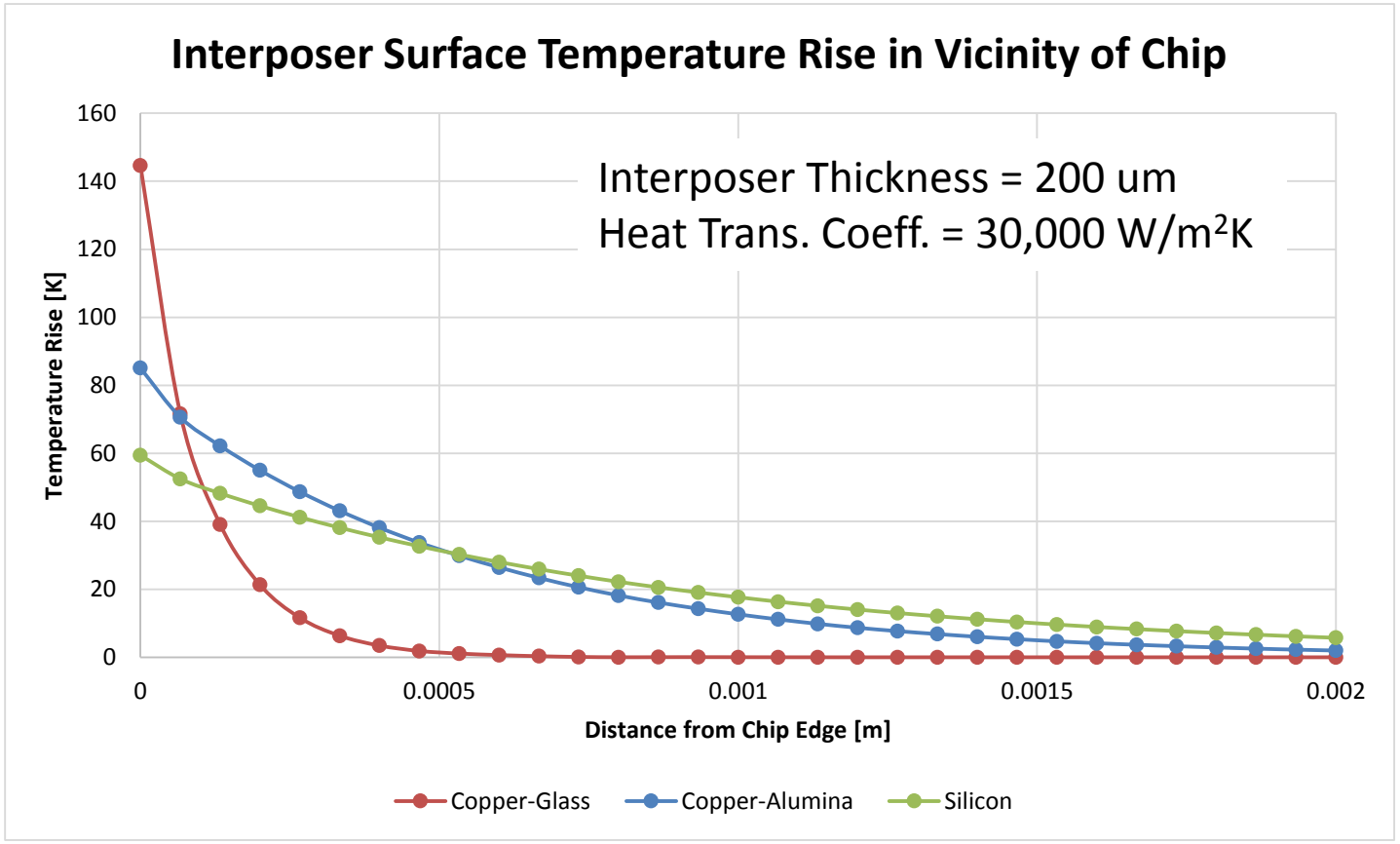
Von Mises stress in copper via and hoop stress in glass substrate

Temperature Mapping using Equivalent Model



- For the analysis, a simplified, one-component isolation model was used.
- A "hot" chip was attached (with die attach layers, not shown) to a via-enhanced interposer with underside convective cooling.
- The homogenized, equivalent model uses anisotropic interposer properties and introduces upper and lower micro-spreading resistances.
- The interposer is assumed to extend far enough beyond the chip to reach a temperature rise of zero (no edge effects, i.e. infinite extent).

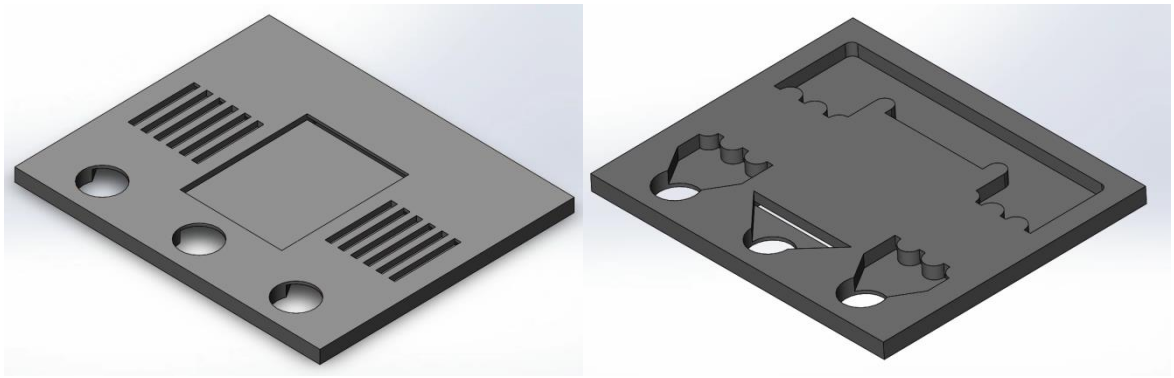
Temperature Mapping using Equivalent Model



By using an equivalent medium for a TXV interposer, package models can be quickly simulated and optimized.

Differential Cooling Analysis

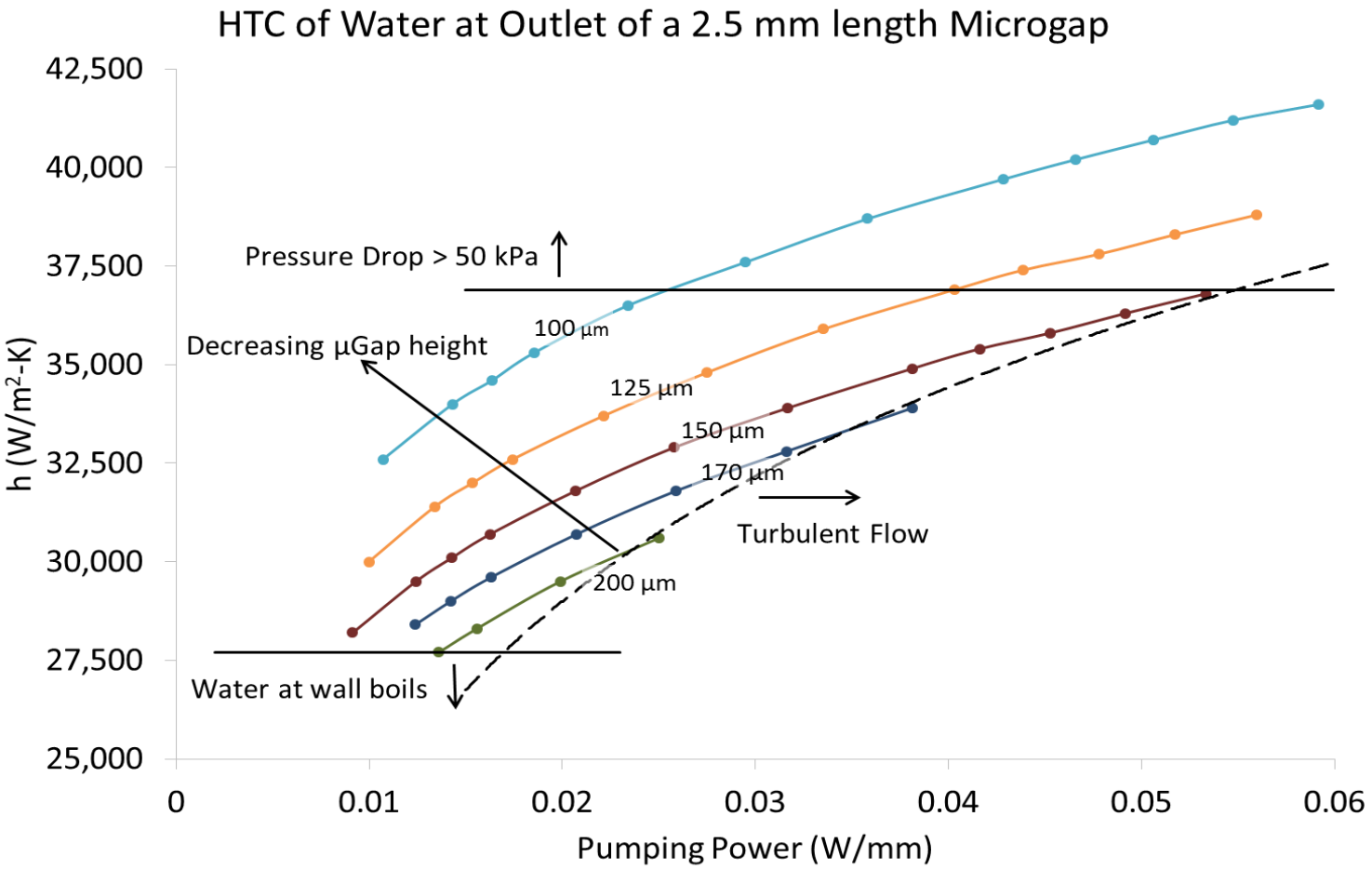
Combining microchannel and microgap coolers can significantly increase COP for the combination as a whole.



Microchannel Coolers		Microgap Coolers	
h [W/m²-K]	Areal Pump Power [W/cm²]	h [W/m²-K]	Areal Pump Power [W/cm²]
115,000 [16]	0.04	15,400 [18]	0.0011
182,000 [17]	0.1	24,000 [18]	0.133
417,000 [17]	10	37,000 (This Research)	1.0

Heat Transfer Coefficients and Pumping Power of Microfluidic Coolers

Microgap Cooler Design



Conclusions

- With a reliable correlation for the effective conductivity of a TXV array, equivalent models for a packages with TXVs can be performed with low computational burden.
- Considering the micro-spreading resistance of a TXV array can lead to optimal via geometry and contact film conductivity and thickness.
- Micro-spreading resistance is minimized by
  - High-aspect vias
  - Fine via pitches
  - Large via pads or even continuous films
  - High-*h*/conductive-contact environments
- Differential microgap/microchannel coolers have been designed for a combination of high COP and high heat transfer.

Acknowledgements

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